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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,860	01/04/2001	Robert S. Mason JR.	EMS-01401	3989

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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	19

DATE MAILED: 01/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,860	MASON ET AL.	
	Examin r	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachm nt(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on October 30, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (USPN: 6,408,370) in view of Dottling (USPN: 6,014,756) and Samra et al. (USPN: 5,809,530).

Regarding claim 1, Yamamoto discloses a data storage system comprising a first disk drive unit (Figure 1, comprised of References 109 and 105); a second disk drive unit, coupled to the first disk drive by a bus (Figure 1, comprised of References 104 and 105); a main cache memory, coupled to the bus (Figure 1, Reference 108 within Reference 104); a secondary memory separate from the main cache memory (comprised of References 107,108 within Reference 109) and provided as part of the first disk drive unit, wherein the secondary memory has at least two sections, a first section used by the first disk drive unit to facilitate disk accesses (Figure 1, Reference 107 within Reference 109; control memory; C 4, L 60-66; the information within the first section of the secondary memory used to facilitate disk accesses is described in C 4, L 14-59) and a second section (Figure 1, Reference 108 within Reference 109) used to cache data

provided to the second section from the second disk drive unit (C 5, L 28-36, L 53-55 – the second disk drive unit provides data, via Reference 104, to the second section of the secondary memory). Yamamoto does not disclose the main cache memory caching data from both the first disk drive and the second disk drive while the second section caches data provided to it from the second disk drive unit, wherein data cached to the secondary memory is different from data cached to the main cache memory. However, Dottling teaches the concept of a main cache memory caching data from both a first and second unit (Figure 1, Reference SHARED CACHE) and parallel caching to two different cache storages (C 5, L 21-23). These features taught by Dottling improves the performance of the system by increasing the effective amount of storage for caching data by caching data in the main cache and another cache and by performing two operations at the same time in oppose to performing operations sequentially. Additionally, Samra teaches the concept of exclusive caches wherein data is stored in one cache at most which means the caches store different data (C 7, L 45-51). Samra teaches that this method of caching provides high effective storage (C 7, L 49-50). Hence it would have been obvious to one of ordinary skill in the art to use the teachings of Dottling and Samra in Yamamoto's system for the desirable purpose of improved performance and effective storage.

Regarding claim 3, Yamamoto discloses a data storage device (Figure 1, comprised of References 100 and 109) comprising a first section of onboard memory containing data for the storage device (Figure 1, Reference 107 within Reference 109; control memory; C 4, L 60-66; the data within the first section of the memory for the storage device is described in C 4, L 14-59); an interface (Figure 1, Reference 103) for communicating data from the data storage device

(from Reference 100 within the data storage device) to the main cache memory a main cache memory (main cache memory - Figure 1, Reference 108 within Reference 104), and a second section of onboard memory associated with the data storage device and used as a cache including data cached from at least one other data storage device, wherein the second section of onboard memory is provided with data from the at least one other data storage device (Figure 1, Reference 108 within Reference 109; C 5, L 11-13, L 28-36, L 53-55 – the at least one other storage device provides data, via Reference 104, to the second section of onboard memory). Yamamoto does not disclose the onboard memory as a volatile memory. The onboard memory in Yamamoto's system is a nonvolatile memory. It is well known in the art to use volatile memory to store data. It is also well known in the art the nonvolatile memory requires data to be erased before overwritten which increases latency, whereas volatile memory can be overwritten without first erasing. Hence, one of ordinary skill in the art would have recognized the benefits afforded by a volatile memory such as reduced latency and would have been motivated to use a volatile memory in Yamamoto's system for the desirable purpose of decreased latency. Additionally, Yamamoto does not disclose the main cache memory containing data from at least one other data storage device and wherein the main cache memory is separate from the data storage device and the at least one other data storage device wherein data cached to the secondary memory is different from data cached to the main cache memory. However, Dottling teaches the concept of a main cache memory caching data from both a first and second unit (Figure 1, Reference SHARED CACHE) and parallel caching to two different cache storages (C 5, L 21-23). These features taught by Dottling improves the performance of the system by increasing the effective amount of storage for caching data by caching data in the main cache and another cache and by

performing two operations at the same time in oppose to performing operations sequentially. Additionally, Samra teaches the concept of exclusive caches wherein data is stored in one cache at most which means the caches store different data (C 7, L 45-51). Samra teaches that this method of caching provides high effective storage (C 7, L 49-50). Hence it would have been obvious to one of ordinary skill in the art to use the teachings of Dottling and Samra in Yamamoto's system for the desirable purpose of improved performance and effective storage.

Regarding claims 4-5, Yamamoto discloses the data storage device as a first disk drive unit (Figure 1, Reference 109 and 105) and the onboard volatile memory includes data cached from at least a second disk drive unit (C 5, L 28-36, L 53-55) and from the first disk drive unit (the first disk drive unit stores data, received by the second disk drive unit, in the onboard memory).

Regarding claims 6-7, Yamamoto discloses an interface that provides and accepts data (inherent – the disk drive control unit, Reference 109 in Figure 1, comprises internal elements which receive inputs and outputs data) and a disk platter that stores data (Figure 1, Reference 105); and a controller that handles communication between the interface and the disk platter, wherein the onboard volatile memory is part of the controller (Figure 1, Reference 109 – internal logic within Reference 109 that handles communication between the interface and the disk platter); a processor of the data storage device (processing element within Reference 109); an other section of onboard volatile memory associated with the data storage device wherein the processor uses the other section of onboard volatile memory in connection with accessing data stored on the

disk platter (Figure 1, Reference 107 within Reference 109; control memory; C 4, L 60-66; the data within the first section of the memory for the storage device is described in C 4, L 14-59).

Regarding claim 8, Yamamoto discloses a first disk drive including a section of onboard memory (Figure 1, onboard memory comprised of References 108 and 107 within Reference 109) associated with the first disk drive (first disk drive is comprised of References 105 and 109 in Figure 1) and including an interface that handles data communication to and from the first disk drive (inherent – the disk drive control unit comprises internal elements which receive inputs and outputs data thereby handling data communication to and from the disk drive); a second disk drive that provides data to the first disk (the second disk drive is comprised of References 104 and 105 in Figure 1; C 5, L 28-30); memory for caching data of the data storage system (Figure 1, memory is comprised of References 108 and 107 within Reference 109 and Reference 108 within Reference 104), the memory including the section of onboard memory associated with the first disk drive wherein the section includes a portion of data cached from at least the second disk drive and wherein data from the second disk drive is provided to the onboard memory (C 5, L 28-36, L 53-55 - the second disk drive provides data, via Reference 104, to the section of onboard memory). Yamamoto does not disclose the main cache memory caching data from both the first disk drive and the second disk drive while the second section caches data provided to it from the second disk drive unit, wherein data cached to the secondary memory is different from data cached to the main cache memory. However, Dottling teaches the concept of a main cache memory caching data from both a first and second unit (Figure 1, Reference SHARED CACHE) and parallel caching to two different cache storages (C 5, L 21-23). These features taught by

Dottling improves the performance of the system by increasing the effective amount of storage for caching data by caching data in the main cache and another cache and by performing two operations at the same time in oppose to performing operations sequentially. Additionally, Samra teaches the concept of exclusive caches wherein data is stored in one cache at most which means the caches store different data (C 7, L 45-51). Samra teaches that this method of caching provides high effective storage (C 7, L 49-50). Hence it would have been obvious to one of ordinary skill in the art to use the teachings of Dottling and Samra in Yamamoto's system for the desirable purpose of improved performance and effective storage.

Regarding claim 9, Yamamoto discloses the onboard memory including a portion of data that is not duplicated elsewhere in the data storage system (Figure 1, Reference 107).

Regarding claim 10, Yamamoto discloses the onboard memory including a portion of data that is duplicated elsewhere in the data storage system (Figure 1, Reference 108).

Regarding claim 11 and 18, Yamamoto discloses the memory for caching including a portion of system memory of the data storage system (inherent – the data storage system is an extension of the system memory and thus is also system memory and therefore, data caching, via the cache also the system memory cache], for the data storage system, inherently caches data of the system memory).

Regarding claim 12, Yamamoto discloses a command generator (comprised of processing unit 100 and unit 140 in Figure 1) that generates at least one command for performing a data operation in connection with caching data of the system memory and at least one command for performing a data operation in connection with caching data of the section of onboard memory (the processing unit stores data in the system memory, 102, when data is retrieved from 105, thereby caching data of the system memory, since the data storage device is an extension of the system memory; and unit 140 writes data to Reference 109, wherein the data is cached in Reference 108 within Reference 109; C 5, L 28-55).

Regarding claim 13, Yamamoto discloses a first command generator (Figure 1, Reference 104 – control logic/software within Reference 104 which operates cache, Reference 108) that generates at least one command for performing a data operation in connection with caching data of the system memory (C 5, L 9-21; data to be written to the data storage system is stored in cache 108, the data storage system is an extension of the system memory and thus the cache caches data of the system memory); and a second command generator (Figure 1, Reference 109 - control logic/software within Reference 109 which operates cache, Reference 108) different from the first command generator that generates at least one command for performing a data operation in connection with caching data of the section of onboard memory (C 5, L 28-55).

Regarding claim 14, Yamamoto discloses a command generator (Figure 1, Reference 109 - control logic/software within Reference 109 which operates cache Reference 108) that generates

at least one command for performing a data operation in connection with data caching of the section of onboard memory (C 5, L 28-30).

Regarding claims 15-17, Yamamoto discloses a host interface unit that includes the command generator (Figure 1, logic within Reference 104 which couples to the host processor(s)), wherein the command generator executes on a dedicated processor (the controller, which comprises the command generator, is a dedicated specialized processor and thus the command generator executes on a dedicated processor), the host interface unit being connected to a host computer (the controller is coupled to the host(s) via channel 103); a disk interface unit for interfacing with the first disk drive (Figure 1, logic within Reference 104 which interfaces to disk drive 105).

Regarding claim 19, Yamamoto discloses a command interpreter that interprets commands in connection with a data caching operation of at least one of the section of onboard memory and the system cache memory (Figure 1, Reference 109 – logic within Reference 109 that receives and executes commands).

Response to Arguments

4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7329.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

KNM

January 5, 2004